WHAT IS CLAIMED IS:

1. A flat panel display, comprising:

a back plate;

cathode and gate electrodes disposed on the back plate and insulated from each other by an insulating layer;

a planar field emission source formed on the cathode electrode;

a grid plate provided with a plurality of apertures corresponding to a pixel area and spaced from the back plate; and

a faceplate spaced from the grid plate and having a screen formed on one surface thereof facing the grid plate.

2. The flat panel display of claim 1, wherein the planar field emission source is formed of a material or mixture of carbonaceous materials selected form the group consisting of carbon nanotube (CNT), fullerene (C_{60}), diamond liked carbon (DLC), and graphite.

3. The flat panel display of claim 1, wherein the grid plate is formed of an insulating substrate.

4. The flat panel display of claim 3, further comprising:

a first grid electrode on a back surface of the grid plate facing the back plate; and

a second grid electrode on a front surface of the grid plate facing the faceplate.

5. The flat panel display of claim 1, wherein the gate electrode is formed on the surface of the back plate, the insulating layer is disposed on the surface of the back plate to cover the gate electrode, and the cathode electrode is formed on the insulating

layer.

6. The flat panel display of claim 5, wherein the gate electrode and the cathode electrode have a structure of plural line patterns and intersect each other at right angles.

7. The flat panel display of claim 5, wherein the gate electrode is formed of a single layer.

8. The flat panel display of claim 5, wherein the planar field emission source is formed on an edge of the cathode electrode.

9. The flat panel display of claim 8, wherein the planar field emission source is formed on a portion of an upper surface and connecting side surface of the cathode electrode.

10. The flat panel display of claim 4, wherein the first grid electrode and the second grid electrode have a structure of plural line patterns along an aperture array.

11. The flat panel display of claim 10, wherein each line pattern of the second grid electrode comprises two sub-electrodes bisected by a line of an aperture array on the grid electrode.

12. The flat panel display of claim 4, wherein the first grid electrode is formed of a single layer.

13. The flat panel display of claim 4, further comprising:

a plurality of first spacers formed on a non-effective area of the back plate for maintaining the space between the back plate and the grid plate; and

a plurality of second spacers formed on a non-effective area of the grid plate for maintaining the space between the grid plate and the faceplate,

wherein an aspect ratio of the second spacers is higher than the first spacers.

14. The flat panel display of claim 1, wherein the grid plate is a mesh electrode.

15. The flat panel display of claim 1, wherein the cathode electrode is formed on the surface of the back plate and having the planar field emission source corresponding to the pixel area, the insulating layer is disposed on the surface of the back plate to cover the cathode electrode except the planar field emission source, and the gate electrode is formed on the insulating layer except the planar field emission source.

16. The flat panel display of claim 15, wherein the gate electrode and the cathode electrode have a structure of plural line patterns and intersect each other at right angles.

17. A method for driving a flat panel display, the flat panel display including a back plate, a gate electrode, a cathode electrode, a planar field emission source formed on the cathode electrode, a grid plate with a first grid electrode and a second grid electrode and having a plurality of apertures corresponding to a pixel area and a faceplate spaced from the grid plate and having a screen formed on one surface thereof facing the grid plate, the method comprising the steps of:

applying scan voltage to the cathode electrode and data signal voltage to the gate electrode to form an electronic field by emitting electrons from the planar field emission source;

applying focus signal voltage to the first grid electrode to converge the electrons at the apertures of the grid plate;

applying deflection signal voltage to the second grid electrode to deflect the electrons passing through the apertures toward target phosphors; and

applying anode signal voltage to the screen to accelerate the electrons to the screen.

18. The method of claim 17, wherein the second grid electrode comprises two sub-electrodes bisected by a line of an aperture array on the grid plate and the two sub-electrodes deflect the electrons using a voltage difference therebetween.

19. A method for driving a flat panel display, the flat panel display including a back plate, a gate electrode, a cathode electrode, a planar field emission source formed on the cathode electrode, a grid plate with a first grid electrode and a second grid electrode and having a plurality of apertures corresponding to a pixel area and a faceplate spaced from the grid plate and having a screen formed on one surface thereof facing the grid plate, the method comprising the steps of:

applying scan voltage to the cathode electrode and data signal voltage to the first grid electrode to form an electric field by emitting electrons from the planar field emission source;

applying field enhancing signal voltage to the gate electrode to enhance the electric field around the planar field emission source;

applying deflection signal voltage to the second grid electrode to deflect the electrons passing through the apertures toward target phosphors; and

applying anode signal voltage to the screen to accelerate the electrons toward the screen.

20. The method of claim 19, wherein the second grid electrode comprises

two sub-electrodes bisected by a line of an aperture array on the grid plate and the two sub-electrodes deflect the electrons using a voltage difference therebetween.

21. A method for driving a flat panel display, the flat panel display including a back plate, a gate electrode, a cathode electrode, a planar field emission source formed on the cathode electrode, a grid plate with a first grid electrode and a second grid electrode and having a plurality of apertures corresponding to a pixel area and a faceplate spaced from the grid plate and having a screen formed on one surface thereof facing the grid plate, the method comprising the steps of:

applying scan voltage to the cathode electrode and data signal voltage to the first grid electrode to form an electric field by emitting electrons from the planar field emission source;

applying field enhancing signal voltage to the gate electrode to enhance the electric field around the planar field emission source;

applying focus signal voltage to the second grid electrode to converge the electrons at the apertures of the grid plate; and

applying anode signal voltage to the screen to accelerate the electrons toward the screen.

22. A method for driving a flat panel display, the flat panel display including a back plate, a gate electrode, a cathode electrode, a planar field emission source formed on the cathode electrode, a mesh plate having a plurality of apertures corresponding to a pixel area, and a faceplate spaced from the grid plate and having a screen formed on one surface thereof facing the mesh plate, the method comprising the steps of;

applying scan voltage to the cathode electrode and data signal voltage to the

gate electrode to form an electric field by emitting electrons from the planar field emission source;

applying focus signal voltage to the mesh plate to converge the electrons at the apertures of the mesh plate; and

applying anode signal voltage to the screen to accelerate the electrons toward the screen.